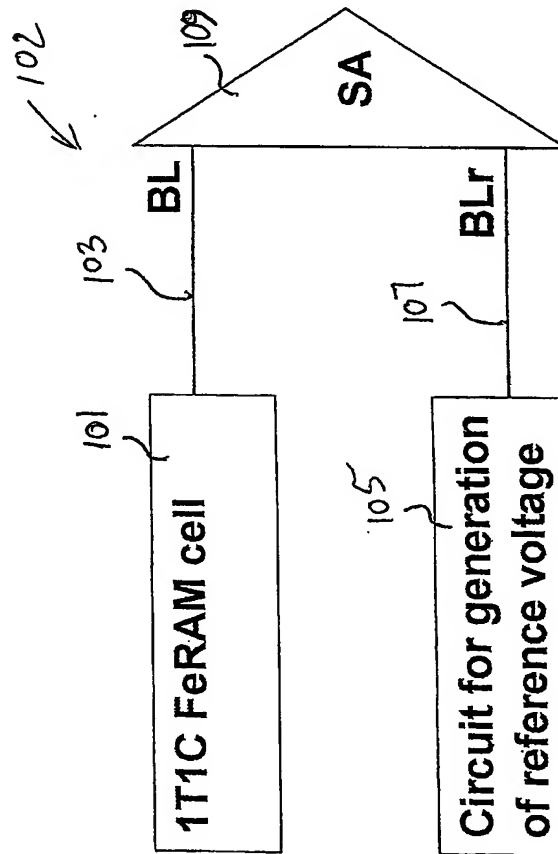


Conventional reference scheme

Sense amplifier compares signals from 1T1C ferroelectric memory cell to a reference signal which is generated, e.g., by use of a non-switched ferroelectric reference capacitor/reference BL of appropriate area/capacitance or by averaging Qsw and Qnsw of two (or more) ferroelectric capacitors

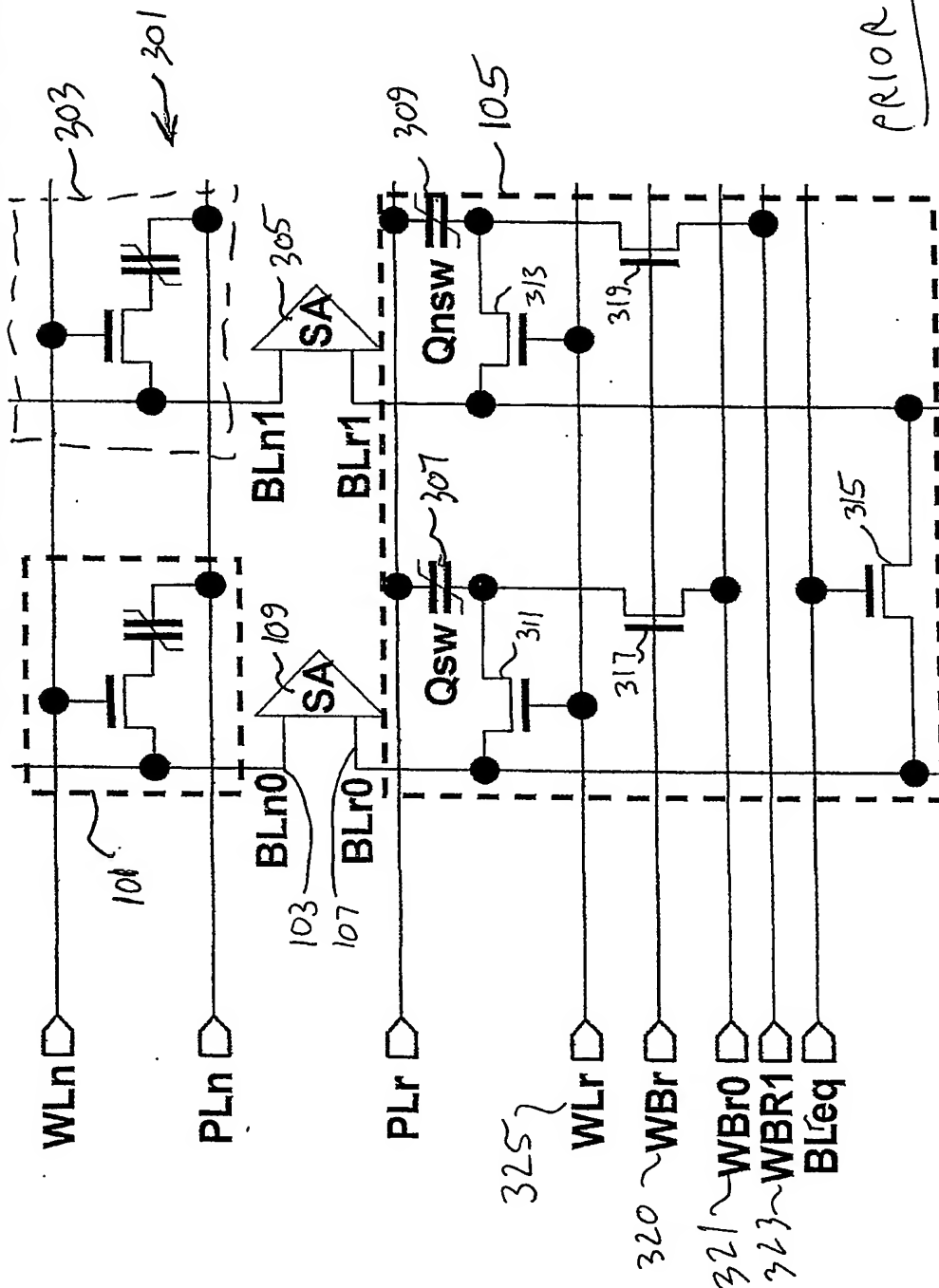


PRIOR - ART

Fig. 1

Second example for conventional reference scheme:
Reference BL voltage by averaging Qsw and Qnsw of ferro caps

1T1C Cell D. Jung et al., IEDM Digest of Technical Papers, p. 279, 1999



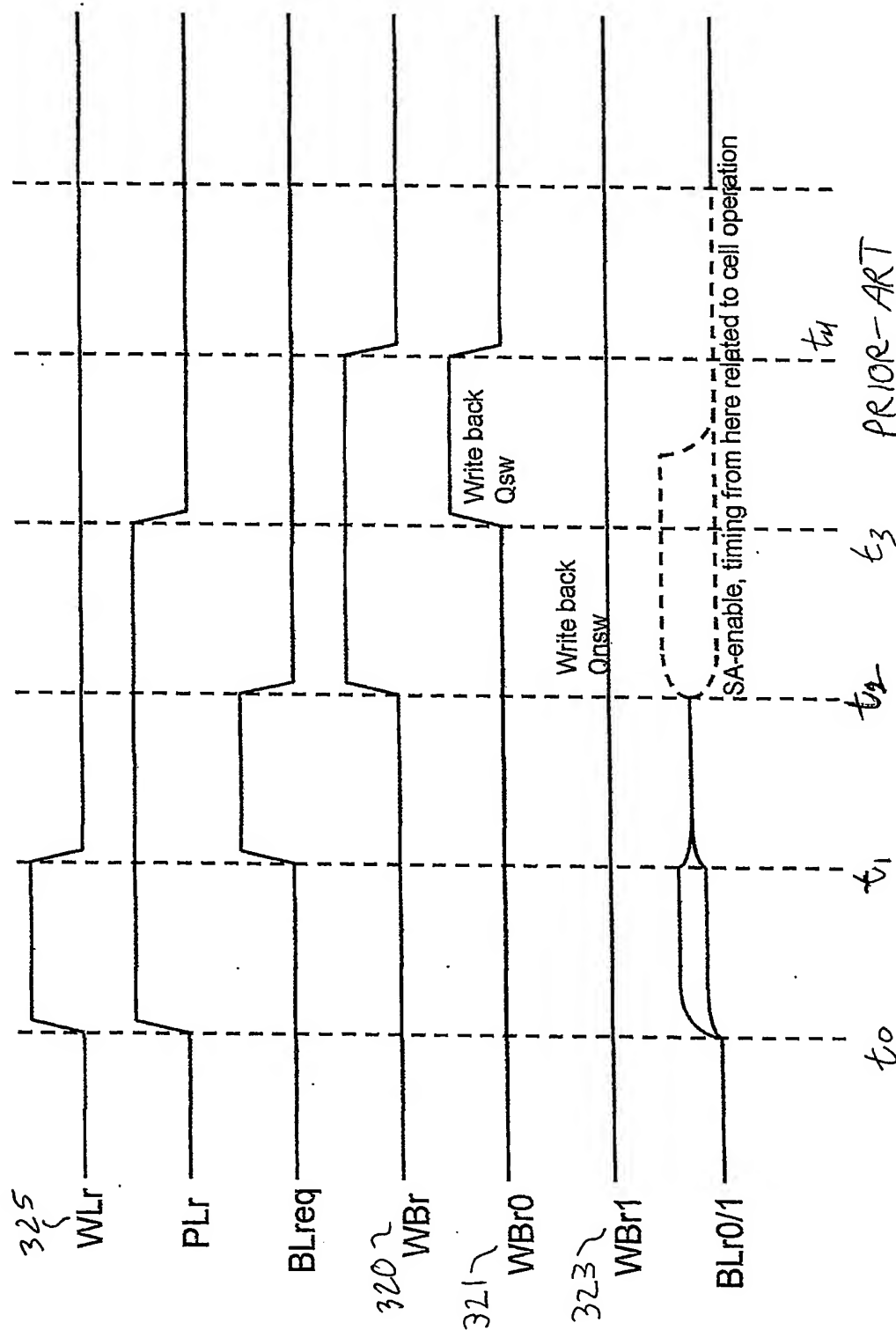
PRIOR-ART

Circuit for generation of reference voltage

Attachment to invention disclosure FDA I 03- 039

FIG. 2

Conventional reference scheme:
example for timing of reference voltage circuit

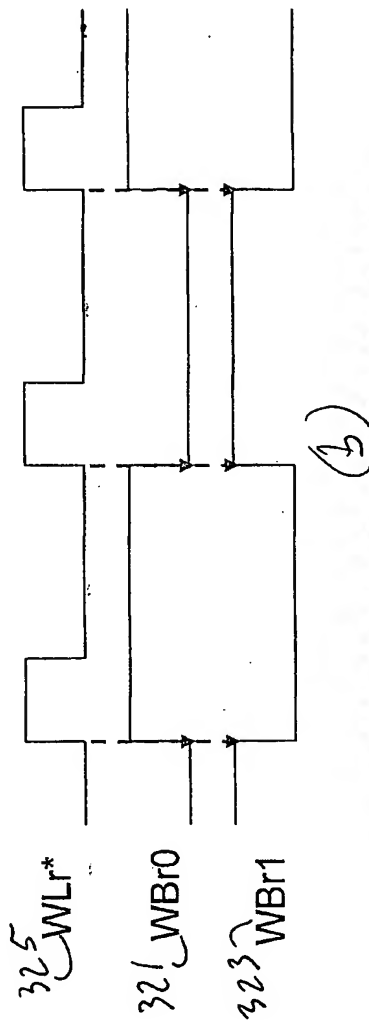
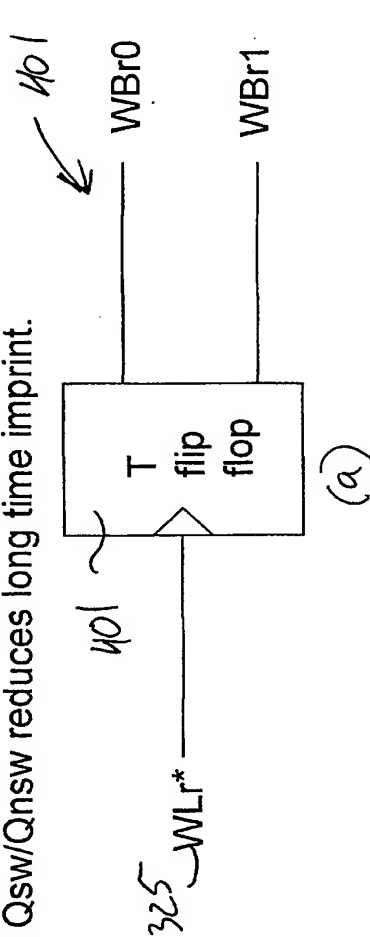


Attachment to invention disclosure FDA I 03- 039

FIG. 3

invention

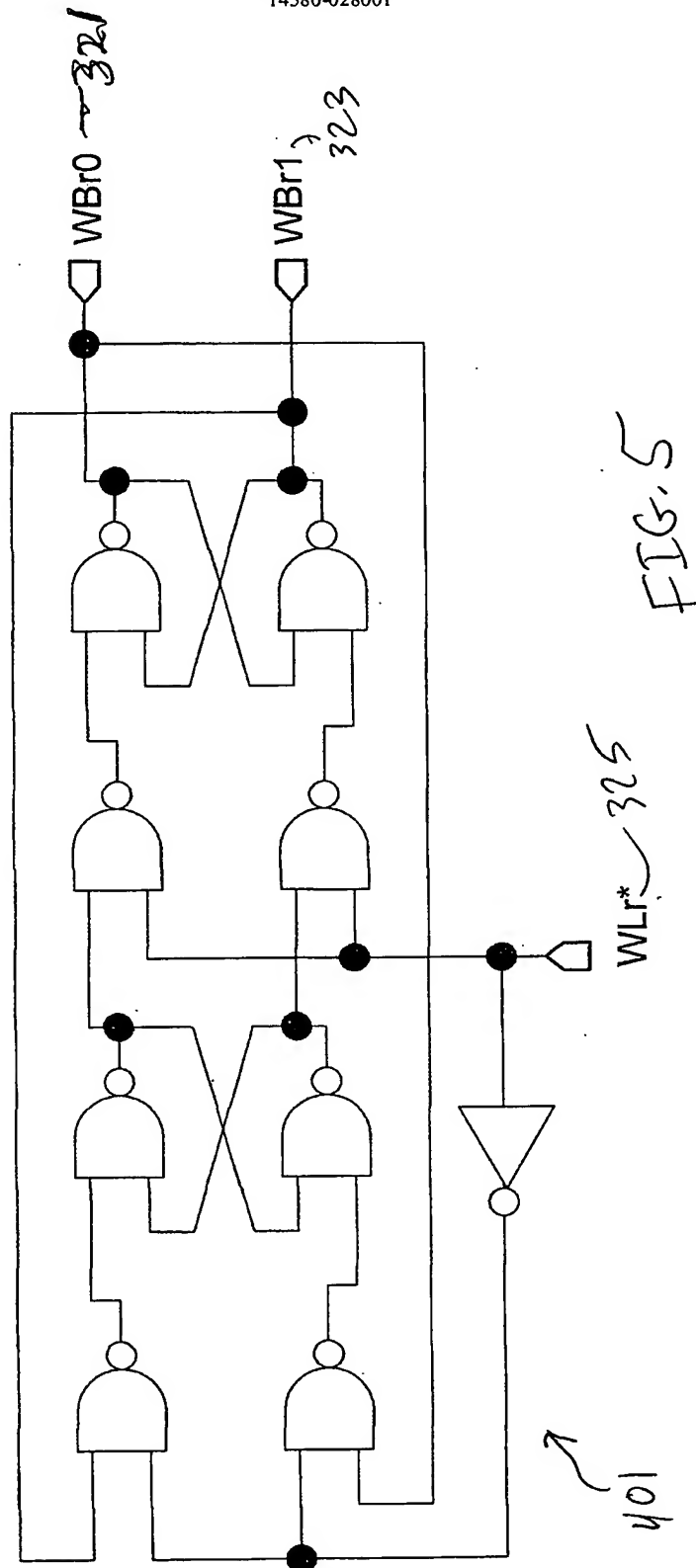
Alternating with each access, Qsw and Qnsw are stored in the ferroelectric reference capacitors.
Background: Fatigue-free PZT is possible, but Imprint-free PZT not.
=> Toggling of Qsw/Qnsw reduces long time imprint.



* Other signals can also be used as trigger signal

FIG. 4

invention: example for toggle flip flop



* Other signals can also be used as trigger signal

invention: example for timing of reference circuit

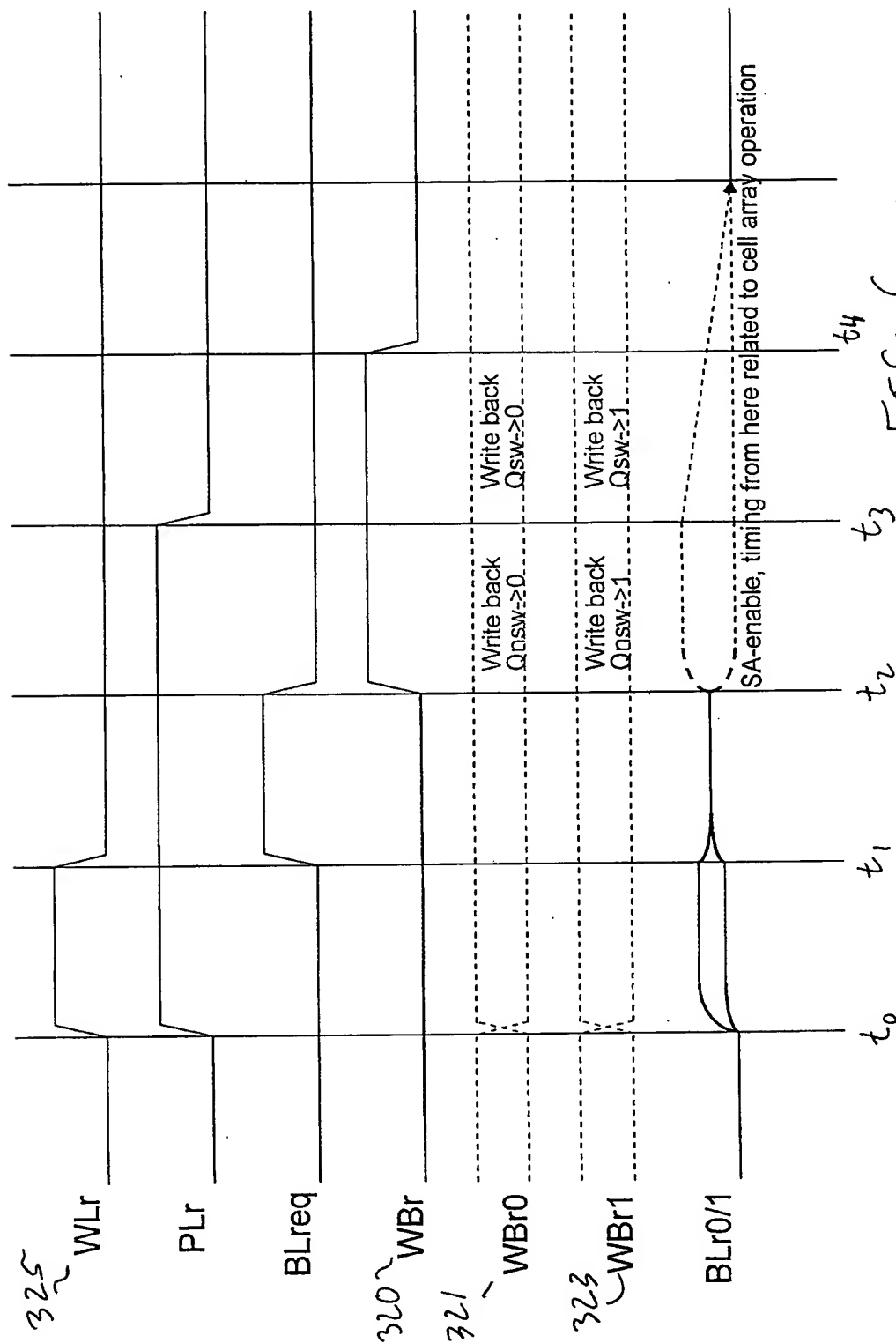


FIG. 6

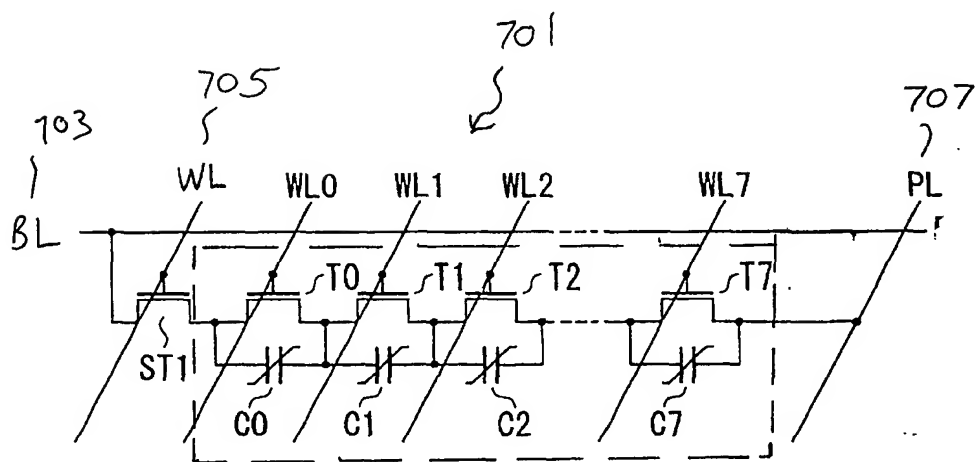


Fig. 7